Amendments to the Specification:

Please amend the Specification as follows.

Please insert the following at Page 3, line 1 of the original application, immediately preceding the paragraph beginning, "FIGURE 4 illustrates. . .":

"FIGURE 3A illustrates a timing diagram showing various signals of the preferred embodiment of FIGURE 3;"

Please insert the following at Page 9, line 29 of the original application, immediately preceding the paragraph beginning, "Now referring to FIGURE 4,. . .":

"Now referring to FIGURE 3A, the reference numeral 370 generally refers to a timing diagram showing various signals of the embodiment as illustrated in FIGURE 3. One skilled in the art will understand that the timing diagram describes the logic states of various signals over an operational time period. As such, one skilled in the art can derive a similar timing diagram based solely on FIGURE 3—depending on the skill of the artisan, a mental timing diagram can be derived that tracks the timing diagram offered in FIGURE 3A. Accordingly, the timing diagram illustrated in FIGURE 3A is offered as a visual aid to understanding, saving time for one skilled in the art seeking to understand the embodiment depicted in FIGURE 3.

Certain assumptions have been made in order to simplify description of the operation of the circuit in FIGURE 3. First, an arbitrary delay time has been selected that is approximately equal to one-half the pulse width of the input clock. Second, the "delay time" as depicted in FIGURE 3A refers to the time it takes for a high-to-low transition at node a0 to propagate through the delay blocks 320-326, through node a20 and inverter 328, to node na20. One skilled in the art will understand that other delay times can also be selected, as described in more detail below. Third, the particular signals shown have been somewhat simplified and depicted as perfectly formed square

waves, as one skilled in the art will understand. As described above, FIGURE 3A is offered in an effort to simplify and aid understanding of the preferred embodiment and the claims thereto.

In particular, FIGURE 3A illustrates an input clock 372. Input clock 372 is a square wave with a pulse width of (t_2-t_1). As illustrated, input clock 372 goes high at time t_1, and low at time t_2. At time t1, when input clock goes high, PMOS 304 and PMOS 310 are turned "on" and NMOS 306 and 310 are turned "off." One skilled in the art will understand that, as used herein, turning "on" or "off" a particular PMOS or NMOS refers to applying the enabling (for "on") or disabling (for "off") gate voltage to the PMOS/NMOS. Generally, one skilled in the art will understand that as depicted, the PMOSes shown are turned "on" when a logic low voltage is applied to their gates, and the NMOSes shown are turned "on" when a logic high voltage is applied to their gates.

At time t1, output clock 373 is also driven high. Output clock 373 is the output signal, "Nckl_out" of inverter 330 of FIGURE 3. As NMOS 312 is on, and PMOS 310 is off, the input to inverter 330, and node a0 376, is low. Additionally, as input clock 372 is high, PMOS 304 is off, and the input to inverter 316 is low. Thus, the output of inverter 316, node nfb, is high and the output of inverter 318, node fb 374, is low.

As illustrated, at time t1 node a0 376 is low. After a delay time, d1, the signal at node a0 propagates through to node na20, on the output side of inverter 328. Thus, at time d1, node na20 378 is high.

At time t2, input clock 372 goes low. As such, NMOS 306 and 312 are off and PMOS 304 and 310 are on. Further, as node fb 374 is low at time t2, PMOS 308 is also on. Thus, node a0 376 goes high (Vdd) and output clock 373 goes low.

At time d2, the transition from low to high at node a0 has propagated to node na20, so node na20 378 goes low. As node na20 378 is low, PMOS 302 is on, and node fb 374 goes high, causing

NMOS 314 to turn on and PMOS 308 to turn off. As node fb 374 goes high, node a0 376 goes low and output clock 373 goes high.

At time t3, input clock 372 goes high. As such, NMOS 306 and 312 are on and PMOS 304 and 310 are off. Time t3 is also time d3, in that the transition from high to low at node a0 has propagated to node na20, so node na20 378 goes high. As such, PMOS 302 turns off, and node fb 374 goes low.

At time t4, input clock 372 goes low. As such, NMOS 306 and 312 are off and PMOS 304 and 310 are on. Further, as node fb 37 is low at time t4, PMOS 308 is also on, and node a0 376 goes high and output clock 373 goes low.

At time d4, the transition from low to high at node a0 has propagated to node na20, so node na20 378 goes low. As node na20 378 is low, PMOS 302 is on, and node fb 374 goes high, causing NMOS 314 to turn on and PMOS 308 to turn off. As node fb 374 goes high, node a0 376 goes low and output clock 373 goes high.

At time t5, input clock 372 goes high. As such, NMOS 306 and 312 are on and PMOS 304 and 310 are off. Time t5 is also time d5, in that the transition from high to low at node a0 has propagated to node na20, so node na20 378 goes high. As such, PMOS 302 turns off, and node fb 374 goes low.

At time t6, input clock 372 goes low. As such, NMOS 306 and 312 are off and PMOS 304 and 310 are on. Further, as node fb 37 is low at time t6, PMOS 308 is also on, and node a0 376 goes high and output clock 373 goes low.

At time d6, the transition from low to high at node a0 has propagated to node na20, so node na20 378 goes low. As node na20 378 is low, PMOS 302 is on, and node fb 374 goes high, causing

NMOS 314 to turn on and PMOS 308 to turn off. As node fb 374 goes high, node a0 376 goes low and output clock 373 goes high.

At time t7, input clock 372 goes high. As such, NMOS 306 and 312 are on and PMOS 304 and 310 are off. Time t7 is also time d7, in that the transition from high to low at node a0 has propagated to node na20, so node na20 378 goes high. As such, PMOS 302 turns off, and node fb 374 goes low.

At time t8, input clock 372 goes low. As such, NMOS 306 and 312 are off and PMOS 304 and 310 are on. Further, as node fb 37 is low at time t8, PMOS 308 is also on, and node a0 376 goes high and output clock 373 goes low.

At time d8, the transition from low to high at node a0 has propagated to node na20, so node na20 378 goes low. As node na20 378 is low, PMOS 302 is on, and node fb 374 goes high, causing NMOS 314 to turn on and PMOS 308 to turn off. As node fb 374 goes high, node a0 376 goes low and output clock 373 goes high.

At time t9, input clock 372 goes high. As such, NMOS 306 and 312 are on and PMOS 304 and 310 are off. Time t9 is also time d9, in that the transition from high to low at node a0 has propagated to node na20, so node na20 378 goes high. As such, PMOS 302 turns off, and node fb 374 goes low.

One skilled in the art will appreciate that the above sequence of events can repeat as often as necessary and/or desired as enabled by the particular circuit depicted in FIGURE 3."